BGT Materials Limited
2.312 Photon Science Institute
University of Manchester
Oxford Road, Manchester,
M13 9PL, United Kingdom

TECHNICAL DATA SHEET

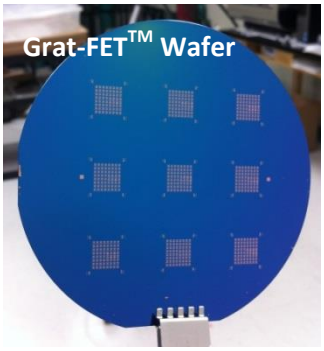
Grat-FET™

Graphene Field-Effect Transistors

BGTM's Grat-FET™ products are state-of-the-art, three-terminal Field-Effect Transistors (FETs) that rely on Bluestone's exclusive, high-mobility CVD graphene. Each Grat-FET™ chip consists of an array of graphene FETs with nine different graphene channel length/width arrangements to accommodate all research and development settings.

Graphene FETs are fabricated on a Si wafer covered with a SiO_2 layer, and the high-mobility Grat-M™ graphene is used as the transistor channel. The graphene transistor consists of three terminals: source and drain metal electrodes contacting the graphene channel and a global back gate enabled by the doped Si substrate. These features facilitate the characteristic ambipolar transport behavior of graphene in the Grat-FETs - achieving both n-type and p-type transport when biased with a proper gate voltage at the substrate.

The product is available as a single chip with 36 FETs or as a 4" wafer that contains 9 chips. As with all Bluestone products, every Grat-FET is tested to ensure our high-quality standards are met.



Device Parameters	
Back-gate oxide	Thermal SiO_2
Back-gate oxide thickness	300 nm
Silicon substrate resistivity	0.001-0.005 Ω-cm
Number of graphene layers	1
Gate leakage current	<0.5 nA (at V_{BG} = 100V)
Channel mobility	2000-3000 cm^2/Vs

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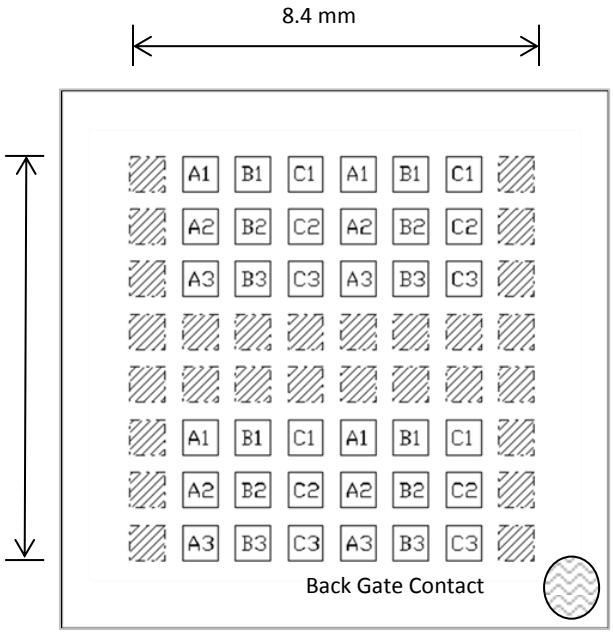
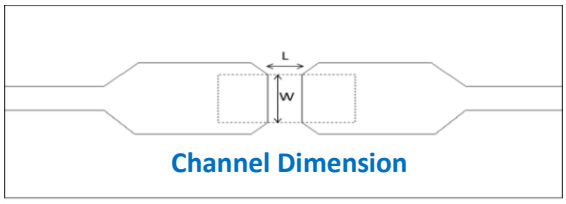
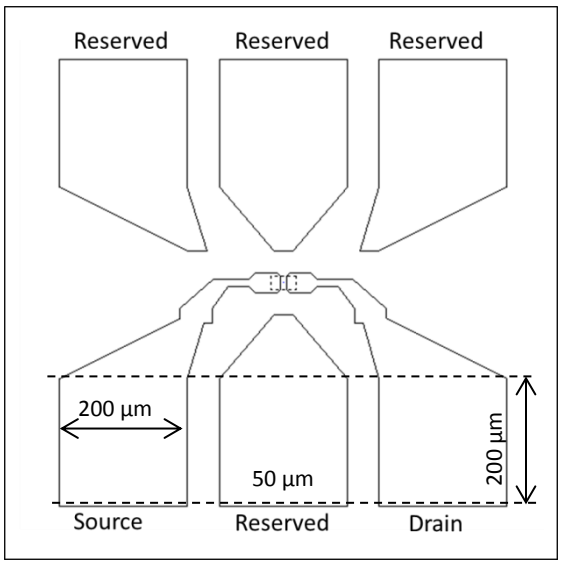
Chip Layout



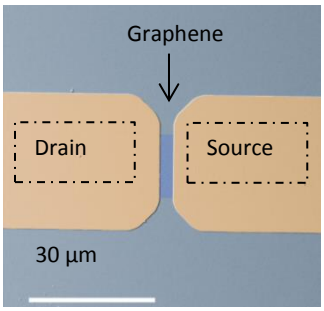
Device type	L (µm)	W (µm)
A1	3	10
A2	5	10
A3	10	10
B1	3	15
B2	5	15
B3	10	15
C1	3	20
C2	5	20
C3	10	20



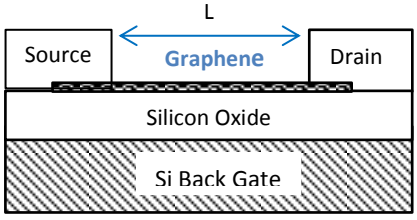
Graphene FET Layout



SEM Image of a Grat-FET Channel



Channel Cross-section



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Electrical Characteristic Curves (Room temperature, Ambient)

Fig. 1 Drain current vs. gate voltage

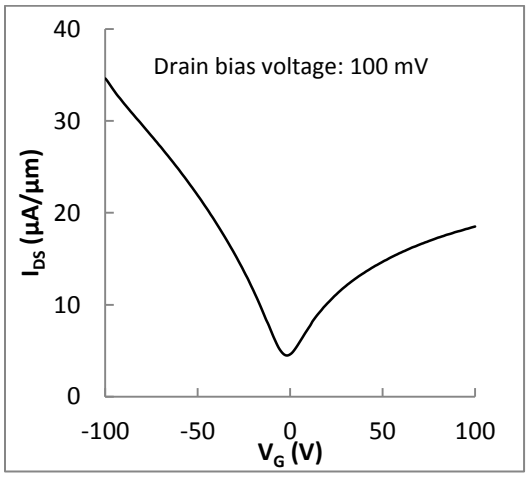
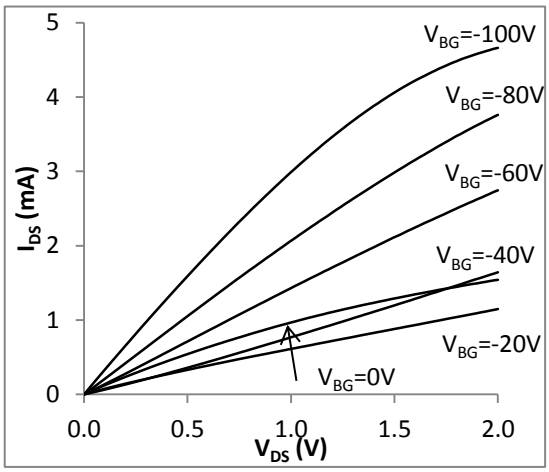


Fig. 2 Drain current vs. drain voltage



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